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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

JRL-550-477



Application Number

10/714,178

Filed

November 17, 2003

First Named Inventor

ORION

Art Unit

2136

Examiner

Daniel L. HOANG.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 33,149
(Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.

Registration number if acting under 37 C.F.R. § 1.34 _____

Signature

John R. Lastova

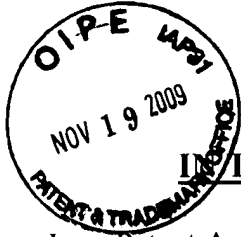
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NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

ORION et al.

Atty. Ref.: 550-477; Confirmation No. 8029

Appl. No. 10/714,178

TC/A.U. 2136

Filed: November 17, 2003

Examiner: Daniel L. HOANG.

For: DIAGNOSTIC DATA CAPTURE CONTROL FOR MULTI-DOMAIN PROCESSORS

* * * * *

November 19, 2009

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Clear Error #1: Gonzales and Kobayashi Fail to Teach All the Independent Claim Features

Claims 1-7 and 10-17 stand rejected as allegedly being obvious in view of Gonzales and newly-applied Kobayashi. This rejection is respectfully traversed.

Gonzales describes a trace function that can operate in two modes. In the first mode, which is known as normal diagnostic mode, the trace function and the CPU are linked together so that the CPU is halted whenever the trace function (i.e., the FIFO) is halted. The trace function is halted in response to an event condition. A user can then examine the contents of the FIFO to determine the flow of software instructions that were executed prior to the event. In the second mode, called a FIFO halt mode, the CPU is not halted when the FIFO is halted to enable real time debug of the CPU. The second mode is used with debugging systems that require real time functionality, e.g., debugging a Hard Disk Drive controller. While the trace function is stopped to allow the debugger to access information from the FIFO, the CPU keeps on running its application. Halting the FIFO could be viewed as “suppressing the capture of diagnostic

data.” Whether the FIFO is halted and the CPU continues to run depends on bits in the control register of the controller. See col. 4, lines 30 – 38 and Table IV. The FIFO may also be halted in response to an event condition. Event conditions are listed in Table II. These conditions are all linked to usual requests (breakpoints, external debug request, trace request). But none is linked to the domain in which the processor is operating. Furthermore, the capturing of diagnostic data is simply stopped in Gonzales by halting the FIFO, it is not suppressed in one domain while being allowed in another.

The combination of Gonzales and Kobayashi, even if it could be made for purposes of argument, fails to disclose or suggest “control logic configured to control said monitoring logic in dependence on said at least one control parameter and the domain in which said processor is operating to suppress capturing of diagnostic data relating to predetermined activities of said processor in said first domain while allowing capturing of diagnostic data relating to predetermined activities of said processor in said second domain,” as recited in claim 1.

The Examiner admits that Gonzales lacks (1) a processor that operates in two different domains and (2) a teaching “that while diagnostic data capture is being suppressed in one domain, capturing of diagnostic data in the second domain is allowed” and relies on Kobayashi.

Kobayashi teaches loading and modifying a computer program without stopping the computer system executing the program. Col. 1, lines 9-12. A reserve memory area stores “additional data codes” when the preliminary space for storing data codes is too small. See claim 4 of Kobayashi. This additional data requiring further storage space is not diagnostic data to be captured by some monitoring logic, but data required by the program to execute correctly. Col. 1, lines 13-21. A computer program requires both instruction and data to execute, and Kobayashi teaches how to increase the storage space of a program (being either storage for instruction or for data) in memory without stopping the computer system. Col. 2, lines 6-8. But

Kobayashi's technology is not related to allowing capture of data in one domain while disabling capture of data in a second domain.

The Examiner points to col. 2, lines 4-27 of Kobayashi as allegedly teaching operating a processor in two different domains and appears to equate the different reserve areas of Kobayashi as the different domains. However, the Examiner does not disclose where or how Kobayashi teaches allowing capture of data in one domain while disabling capture of data in a second domain.

Thus, even if Kobayashi and Gonzales could be combined as suggested by the Examiner, i.e., "when a program needs to be modified to incorporate additional functions or to remove errors...", the data stored in the different reserve areas in such a modified Gonzales system would not be the claimed diagnostic data but instead would be data required to modify the program. The claims define diagnostic data as being data captured by monitoring logic monitoring the processor in response to performing a trace or debug function. Such diagnostic data is not related to the data required by a program to execute correctly. Indeed, diagnostic data is related to diagnosing the actual program execution. Consequently, the combination of Gonzales and Kobayashi does not disclose "suppress[ing] capturing of diagnostic data relating to predetermined activities of said processor in said first domain while allowing capturing of diagnostic data relating to predetermined activities of said processor in said second domain."

In contrast to Gonzales and Kobayashi, the claimed technology selectively stops the monitoring logic from capturing data relating to the activities of the processor when the processor is operating in a given domain. Such a domain may be for example a secure domain or any domain where it is desired to prevent processor activity from being monitored by an external debugger. The condition to suppress the capturing of data is hence related to the domain the processor is running in, and not just to usual debug events as in Gonzales.

The claimed technology addresses and solves the problem of data leaking between domains during diagnostic monitoring by enabling suppression of data capture one domain while allowing it in another. Gonzales and Kobayashi are not concerned with this data leakage problem between domains. Instead, Gonzales allows trace data to be output from a processor while the CPU is still functioning, and Kobayashi allows modification of a control program with stopping execution of that control program. Neither reference is concerned with data leakage between domains.

Claim 1 also recites “a storage element configured to store at least one control parameter.” The Examiner refers to col. 3, lines 29 – 32 of Gonzales for this feature. This text describes a SERIAL I/O signal that is received by the controller, but it does not disclose that the SERIAL I/O signal is stored in a storage element. Instead, the SERIAL I/O signal directs the controller to either halt the CPU and the FIFO or just halt the FIFO depending on the signals received. Thus, this section does not disclose a storage element for storing the claimed control parameter.

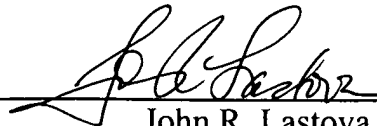
Clear Error #2: Gonzales Fails to Teach the Features of Claims 2 and 11

The Examiner maintains the rejection of claims 2 and 11 based on Gonzales. The Examiner equates the normal diagnostic mode (CPU and FIFO halted) in Gonzales as the claimed non-secure mode and the FIFO halt mode (FIFO halted and CPU running) in Gonzales as the claimed secure mode. But there is no indication of what the Examiner considers to be the secure domain and the non-secure domain in Gonzales. In fact, the claimed domains are not disclosed in Gonzales, as admitted by the Examiner on page 3 of the final rejection.

The final rejection is improper and should be withdrawn. Accordingly, the application is in condition for allowance. The Examiner is also requested to acknowledge consideration of the information submitted in the IDS filed on April 19, 2007.

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Respectfully submitted,
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